# RAMAKRISHNA MISSION VIDYAMANDIRA

**(Residential Autonomous College affiliated to University of Calcutta)**

**FIRST YEAR [2015-18]**

**B.A./B.Sc. FIRST SEMESTER (July – December) 2015**

**Mid-Semester Examination, September 2015**

Date : 14/09/2015 — **COMPUTER SCIENCE (Honours)**

Time : 11 am – 1 pm — Paper : I — Full Marks : 50

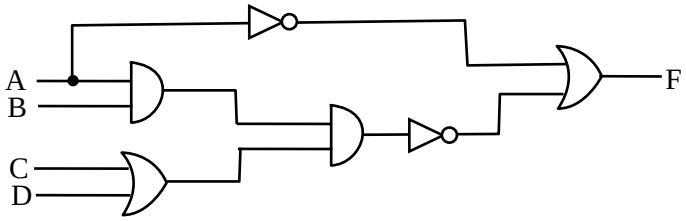
**[Use a separate Answer Book for each group]**

## Group – A

(*Answer **any one** question*) [1×15]

1. a) Encode data bits 10110 using Hamming code considering odd parity. [3]
   b) Find the minimal POS expression for the following using Quine-McCluskey method. $\Pi M(2,3,8,12,13)\cdot\Pi d(10,14)$ [5]
   c) Prove transposition theorem of boolean algebra using boolean laws and axionms. [2]
   d) Subtract $(1110\cdot001)_2$ from $(1000\cdot0101)_2$. [2]
   e) Add $-25\cdot125_{10}$ with $-28\cdot625_{10}$ using 12-bit 2's complement arithmetic. [3]

2. a) Demorganize : $\overline{\overline{AB}(\overline{C}\overline{D}+\overline{E}F)(\overline{AB}+\overline{CD})}$ [3]
   b) Convert the following logic circuit in NOR universal logic. [3]




   c) Express the function $Y = A + \overline{B}C$ in canonical POS form. [3]
   d) Subtract $106\cdot5_{10}$ from $759\cdot2_{10}$ in 8421 BCD code using 10's complement method. [2·5]
   e) 'Roman number system is non-positional' —Justify. [2]
   f) Explain how parity is useful in error detection. [1·5]

## Group – B

3. Answer **any one** question : [1×5]
   a) Explain the function of a priority encoder of your choice. Draw its logic diagram showing its truth table. [2+3]
   b) Evaluate $X = ((A + B) * C) / D$ using one address and zero address instruction format. [5]

Answer **any three** questions : [3×10]

4. a) Realize a D Flip-Flop using J-K Flip-Flop. [3]
   b) Realize a 16:1 Mux using two 8:1 Mux and explain its operation. [2+2]
   c) Realize the following boolean function using a 8:1 multiplexer. [3]
   $F(w, x, y, z) = \sum m(1,3,5,7,13,14,15)$

5. a) Design a 2-bit magnitude comparator circuit and explain its operation. [3+2]
   b) How does master-slave flip-flop avoid race-around condition? [2]
   c) Design a gray code to binary code converter circuit. [3]

6. a) Draw and explain the instruction cycle. [6]
   b) Compare Von neumann and Harvard architecture. [4]

7. a) Realize a 4×4 RAM using 1×1 RAM. [5]

   b) Suppose a cache has 256 lines with 16 words. Main memory size is 64K. Show the address format using (i) Direct mapping and (ii) Associative mapping. [5]

8. a) What is cache coherency? [2]

   b) Compare synchronous and asynchronous data transfer. [3]

   c) Explain the IEEE standard for representing floating point number. [5]

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